

Features

- High-density, High-performance, Electrically-erasable Complex Programmable Logic Device
 - 64 Macrocells
 - 5 Product Terms per Macrocell, Expandable up to 40 per Macrocell
 - 44, 68, 84, 100 Pins
 - 7.5 ns Maximum Pin-to-pin Delay
 - Registered Operation up to 125 MHz
 - Enhanced Routing Resources
- In-System Programmability (ISP) via JTAG
- Flexible Logic Macrocell
 - D/T/Latch Configurable Flip-flops
 - Global and Individual Register Control Signals
 - Global and Individual Output Enable
 - Programmable Output Slew Rate
 - Programmable Output Open Collector Option
 - Maximum Logic Utilization by Burying a Register with a COM Output
- Advanced Power Management Features
 - Automatic μ A Standby for “L” Version
 - Pin-controlled 1 mA Standby Mode
 - Programmable Pin-keeper Circuits on Inputs and I/Os
 - Reduced-power Feature per Macrocell
- Available in Commercial and Industrial Temperature Ranges
- Available in 44-, 68-, and 84-lead PLCC; 44- and 100-lead TQFP; and 100-lead PQFP
- Advanced EE Technology
 - 100% Tested
 - Completely Reprogrammable
 - 10,000 Program/Erase Cycles
 - 20-year Data Retention
 - 2000V ESD Protection
 - 200 mA Latch-up Immunity
- JTAG Boundary-scan Testing to IEEE Std. 1149.1-1990 and 1149.1a-1993 Supported
- PCI-compliant
- 3.3V or 5.0V I/O Pins
- Security Fuse Feature
- Green (Pb/Halide-free/RoHS Compliant) Package Options

Enhanced Features

- Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)
- Output Enable Product Terms
- Transparent – Latch Mode
- Combinatorial Output with Registered Feedback within Any Macrocell
- Three Global Clock Pins
- ITD (Input Transition Detection) Circuits on Global Clocks, Inputs and I/O
- Fast Registered Input from Product Term
- Programmable “Pin-keeper” Option
- V_{CC} Power-up Reset Option
- Pull-up Option on JTAG Pins TMS and TDI
- Advanced Power Management Features
 - Edge-controlled Power-down “L”
 - Individual Macrocell Power Option
 - Disable ITD on Global Clocks, Inputs and I/O



**High-
performance
Complex
Programmable
Logic Device**

**ATF1504AS
ATF1504ASL**





Description

The ATF1504AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504AS's enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504AS has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504AS allows fast, efficient generation of complex logic functions. The ATF1504AS contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504AS macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V _{CCINT} or V _{CCIO} (5V) Power Supply	5V ± 5%	5V ± 10%
V _{CCIO} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V

DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units	
I _{IL}	Input or I/O Low Leakage Current	V _{IN} = V _{CC}		-2	-10	μA	
I _{IH}	Input or I/O High Leakage Current			2	10		
I _{OZ}	Tri-state Output Off-state Current	V _O = V _{CC} or GND	-40		40	μA	
I _{CC1}	Power Supply Current, Standby	V _{CC} = Max V _{IN} = 0, V _{CC}	Std Mode	Com.	105		mA
				Ind.	130		mA
			"L" Mode	Com.	10		μA
				Ind.	10		μA
I _{CC2}	Power Supply Current, Power-down Mode	V _{CC} = Max V _{IN} = 0, V _{CC}	"PD" Mode	1	10	mA	
I _{CC3} ⁽²⁾	Current in Reduced-power Mode	V _{CC} = Max V _{IN} = 0, V _{CC}	Std Power	Com	85		ma
				Ind	105		
V _{CCIO}	Supply Voltage	5.0V Device Output	Com.	4.75		5.25	V
			Ind.	4.5		5.5	V
V _{CCIO}	Supply Voltage	3.3V Device Output		3.0		3.6	V
V _{IL}	Input Low Voltage		-0.3		0.8	V	
V _{IH}	Input High Voltage		2.0		V _{CCIO} + 0.3	V	
V _{OL}	Output Low Voltage (TTL)	V _{IN} = V _{IH} or V _{IL} V _{CCIO} = MIN, I _{OL} = 12 mA	Com.			0.45	V
			Ind.				
	Output Low Voltage (CMOS)	V _{IN} = V _{IH} or V _{IL} V _{CC} = MIN, I _{OL} = 0.1 mA	Com.			.2	V
			Ind.			.2	V
V _{OH}	Output High Voltage (TTL)	V _{IN} = V _{IH} or V _{IL} V _{CCIO} = MIN, I _{OH} = -4.0 mA		2.4		V	

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. When macrocell reduced-power feature is enabled.

Pin Capacitance

	Typ	Max	Units	Conditions
C _{IN}	8	10	pF	V _{IN} = 0V; f = 1.0 MHz
C _{I/O}	8	10	pF	V _{OUT} = 0V; f = 1.0 MHz

- Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.
The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Absolute Maximum Ratings*

Temperature Under Bias.....	-40°C to +85°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-2.0V to +7.0V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V ⁽¹⁾
Programming Voltage with Respect to Ground.....	-2.0V to +14.0V ⁽¹⁾

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7.0V for pulses of less than 20 ns.

AC Characteristics

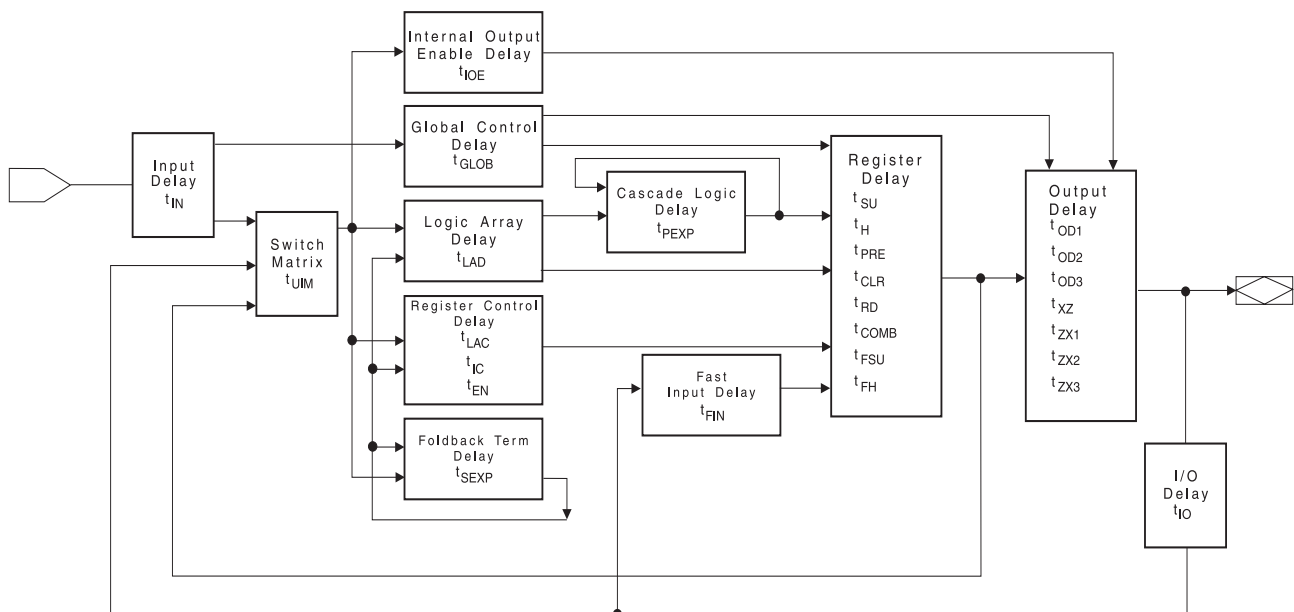
Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		20		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		16		25	ns
t_{SU}	Global Clock Setup Time	6		7		11		16		20		ns
t_H	Global Clock Hold Time	0		0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		3		5		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1.0		1.5		2		ns
t_{COP}	Global Clock to Output Delay		4.5		5		8		10		13	ns
t_{CH}	Global Clock High Time	3		4		5		6		7		ns
t_{CL}	Global Clock Low Time	3		4		5		6		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		5		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		20		25	ns
t_{ACH}	Array Clock High Time	3		4		6		8		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		8		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		17		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		66		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		17		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		66		50		MHz

AC Characteristics (Continued)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	166.7		125		100		83.3		60		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		10		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		1		1.2	ns
t_{LAD}	Logic Array Delay		3		5		6		7		8	ns
t_{LAC}	Logic Control Delay		3		5		6		7		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		3		4	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{CCIO} = 5V; C_L = 35\text{ pF}$)		2		1.5		4		5		6	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V; C_L = 35\text{ pF}$)		2.5		2.0		5		6		7	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; $V_{CCIO} = 5V\text{ or }3.3V; C_L = 35\text{ pF}$)		5		5.5		8		10		10	ns

Note: See ordering information for valid part numbers.

Timing Model

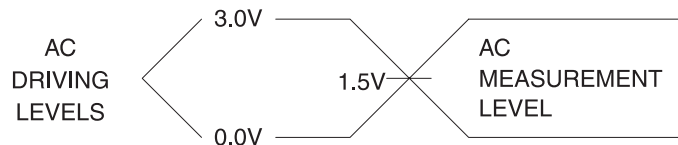


AC Characteristics (Continued)

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 5.0V$; $C_L = 35$ pF)		4.0		5.0		7		9		10	ns
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; $V_{CCIO} = 3.3V$; $C_L = 35$ pF)		4.5		5.5		7		9		10	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; $V_{CCIO} = 5.0V/3.3V$; $C_L = 35$ pF)		9		9		10		11		12	ns
t_{XZ}	Output Buffer Disable Delay ($C_L = 5$ pF)		4		5		6		7		8	ns
t_{SU}	Register Setup Time	3		3		4		5		6		ns
t_H	Register Hold Time	2		3		4		5		6		ns
t_{FSU}	Register Setup Time of Fast Input	3		3		2		2		3		ns
t_{FH}	Register Hold Time of Fast Input	0.5		0.5		2		2		2.5		ns
t_{RD}	Register Delay		1		2		1		2		2	ns
t_{COMB}	Combinatorial Delay		1		2		1		2		2	ns
t_{IC}	Array Clock Delay		3		5		6		7		8	ns
t_{EN}	Register Enable Time		3		5		6		7		8	ns
t_{GLOB}	Global Control Delay		1		1		1		1		1	ns
t_{PRE}	Register Preset Time		2		3		4		5		6	ns
t_{CLR}	Register Clear Time		2		3		4		5		6	ns
t_{UIM}	Switch Matrix Delay		1		1		2		2		2	ns
t_{RPA}	Reduced-power Adder ⁽²⁾		10		11		13		14		15	ns

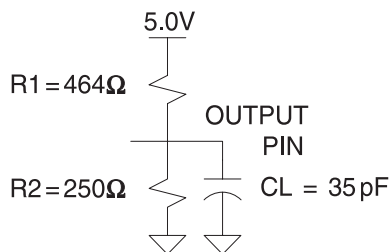
- Notes: 1. See ordering information for valid part numbers.
 2. The t_{RPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{TIC} , t_{ACL} , and t_{SEXP} parameters for macrocells running in the reduced-power mode.

Input Test Waveforms and Measurement Levels



t_R , $t_F = 1.5$ ns typical

Output AC Test Loads



Note: *Numbers in parenthesis refer to 3.0V operating conditions (preliminary).

Power-down Mode

The ATF1504AS includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 10 mA. During power-down, all output data and internal logic states are latched internally and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down mode feature is enabled in the logic design file or as a fitted or translated s/w option. Designs using the power-down pin may not use the PD pin as a logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Power Down AC Characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	-7		-10		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid I, I/O before PD High	7		10		15		20		25		ns
t_{GVDH}	Valid OE ⁽²⁾ before PD High	7		10		15		20		25		ns
t_{CVDH}	Valid Clock ⁽²⁾ before PD High	7		10		15		20		25		ns
t_{DHIX}	I, I/O Don't Care after PD High		12		15		25		30		35	ns
t_{DHGX}	OE ⁽²⁾ Don't Care after PD High		12		15		25		30		35	ns
t_{DHCX}	Clock ⁽²⁾ Don't Care after PD High		12		15		25		30		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1	μs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	μs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	μs
t_{DLOV}	PD Low to Valid Output		1		1		1		1		1	μs

- Notes:
1. For slow slew outputs, add t_{SSO} .
 2. Pin or product term.
 3. Includes t_{RPA} due to reduced power bit enabled.

PCI DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V _{CC}	Supply Voltage		4.75	5.25	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{IL}	Input Low Voltage		-0.5	0.8	V
I _{IH}	Input High Leakage Current	V _{IN} = 2.7V		70	μA
I _{IL}	Input Low Leakage Current	V _{IN} = 0.5V		-70	μA
V _{OH}	Output High Voltage	I _{OUT} = -2 mA	2.4		V
V _{OL}	Output Low Voltage	I _{OUT} = 3 mA, 6 mA		0.55	V
C _{IN}	Input Pin Capacitance			10	pF
C _{CLK}	CLK Pin Capacitance			12	pF
C _{IDSEL}	IDSEL Pin Capacitance			8	pF
L _{PIN}	Pin Inductance			20	nH

Note: Leakage current is with pin-keeper off.

PCI AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
I _{OH(AC)}	Switching Current High (Test High)	0 < V _{OUT} ≤ 1.4	-44		mA
		1.4 < V _{OUT} < 2.4	-44+(V _{OUT} - 1.4)/0.024		mA
		3.1 < V _{OUT} < V _{CC}		Equation A	mA
		V _{OUT} = 3.1V		-142	μA
I _{OL(AC)}	Switching Current Low (Test Point)	V _{OUT} > 2.2V	95		mA
		2.2 > V _{OUT} > 0	V _{OUT} /0.023		mA
		0.1 > V _{OUT} > 0		Equation B	mA
		V _{OUT} = 0.71		206	mA
I _{CL}	Low Clamp Current	-5 < V _{IN} ≤ -1	-25+(V _{IN} + 1)/0.015		mA
SLEW _R	Output Rise Slew Rate	0.4V to 2.4V load	0.5	3	V/ns
SLEW _F	Output Fall Slew Rate	2.4V to 0.4V load	0.5	3	V/ns

Notes: 1. Equation A: I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45) for V_{CC} > V_{OUT} > 3.1V.
 2. Equation B: I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT}) for 0V < V_{OUT} < 0.71V.



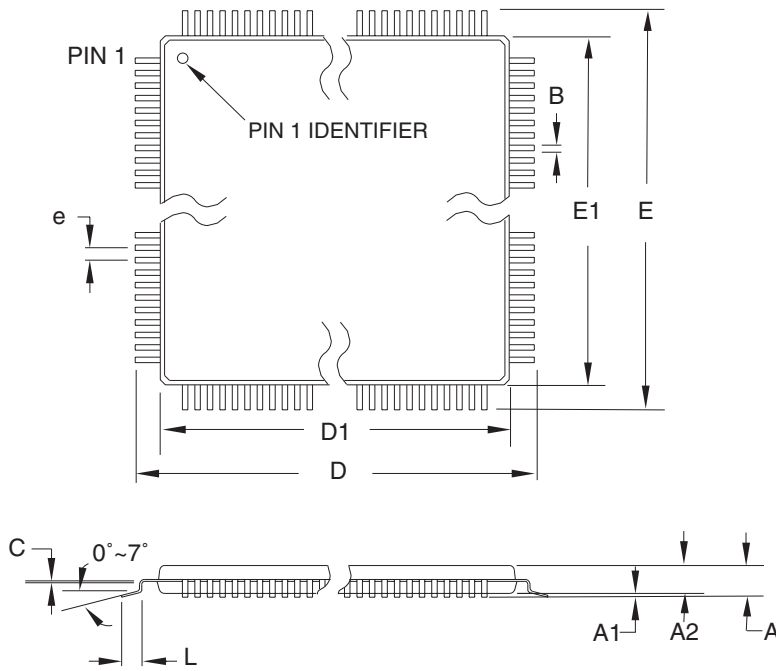
ATF1504AS Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1504AS-7 AX44 ATF1504AS-7 JX44	44A 44J	Commercial (0°C to 70°C)
10	5	125	ATF1504AS-10 AU44 ATF1504AS-10 JU44 ATF1504AS-10AU100 ATF1504AS-10 JU84	44A 44J 100A 84J	Industrial (-40°C to +85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
68J	68-lead, Plastic J-leaded Chip Carrier (PLCC)
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q1	100-lead, 14 x 20 mm Body, Plastic Quad Flat Package (PQFP)
100A	100-lead, 14 x 14 mm Body, Thin Profile Plastic Quad Flat Package (TQFP)

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.